

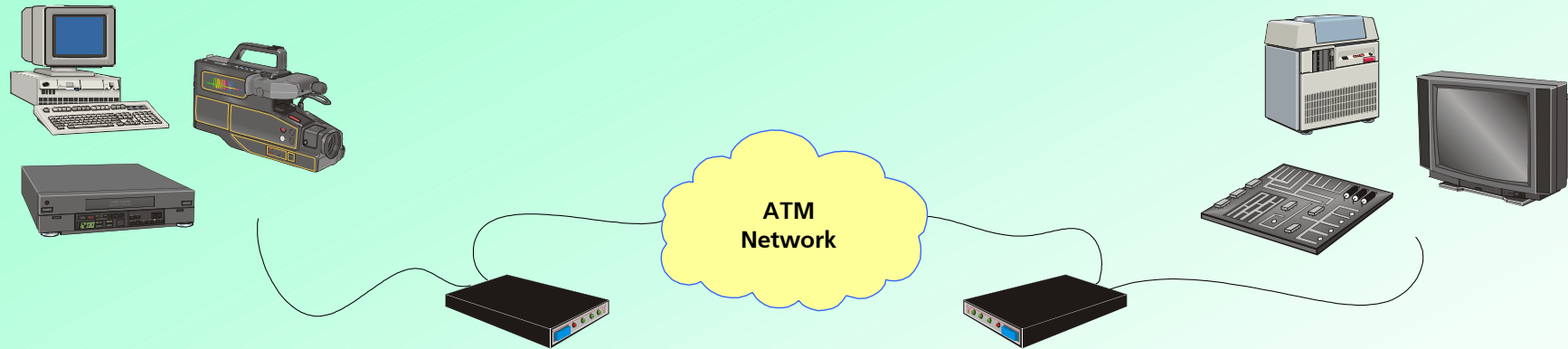
A Prototype of an AAL for High Bit Rate Real-Time Data Transmission Systems over ATM Networks using a RSE CODEC

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Structure

- 1. Motivation**
- 2. FEC system**
- 3. FEC with RSE CODEC**
- 4. Prototype**
- 5. Summary**

Studio/Video Applications



➤ data-rate up to 300MBit/s

➤ no lossy compression

➤ no errors acceptable

➤ no retransmission

Motivation

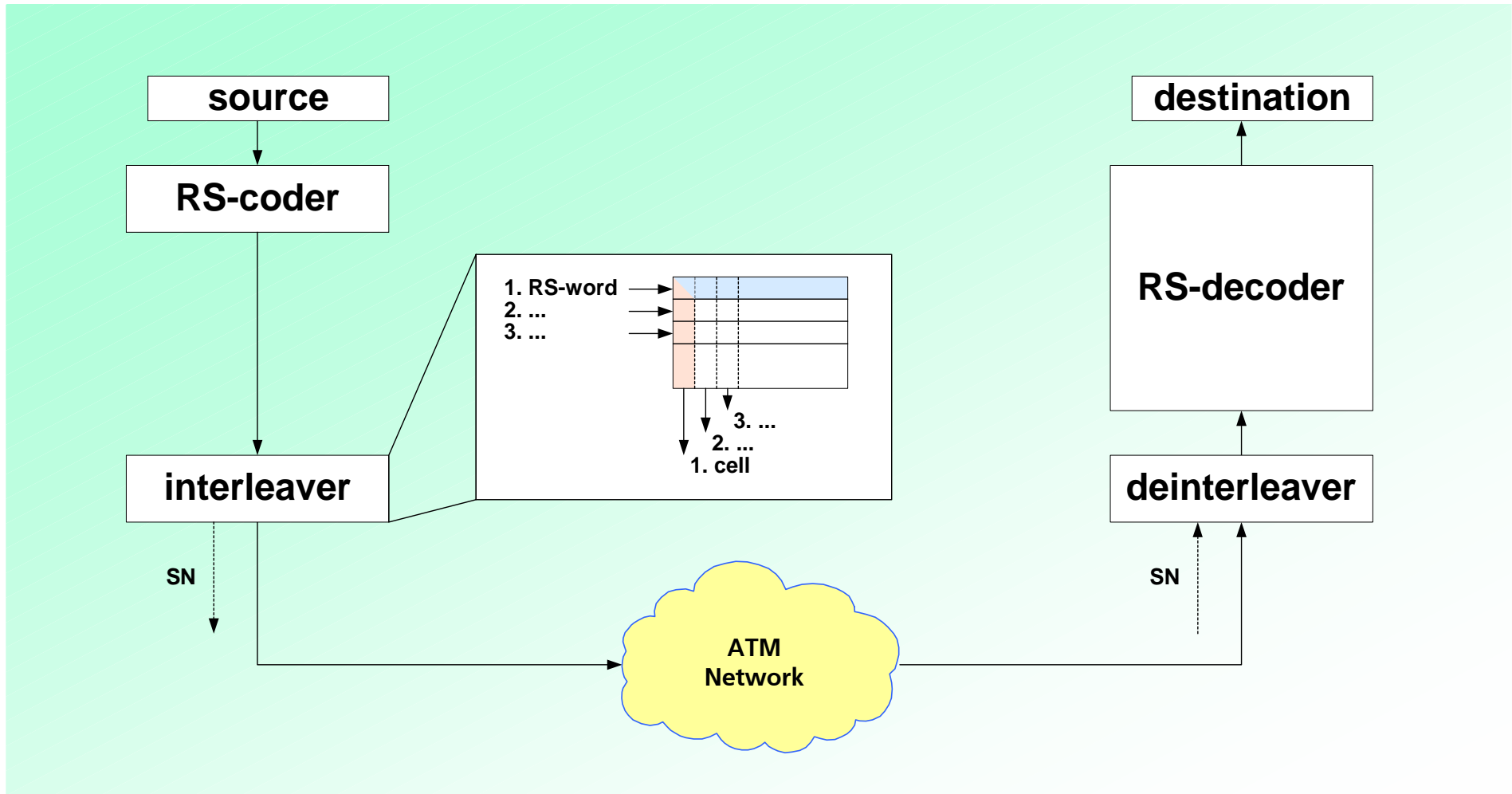
Studio/Video Applications :

- high bit-rate real-time environment
- not fault-tolerant towards bit-errors and packet-losses

Data Transmission systems :

- packet-losses
- low bit-error-rate

FEC System



Reed-Solomon-Decoding

- **Syndrome Calculation**

$$S_i = r(\alpha^i) \text{ with } i \in [1..2t]$$

- **Error-Location-Polynomial**
(Berlecamp-Massey / Euklid)

$$\sigma(x) = \prod_{i=1}^v (1 + \beta_i x) = 1 + \sigma_1 x + \dots + \sigma_v x^v$$

- **Chien-Search**

$$I = \{i \mid \sigma(\alpha^{-i}) = 0\} = j_1, \dots, j_v \text{ with } \beta_l = \alpha^{j_l}$$

- **Error-Value-Polynomial**

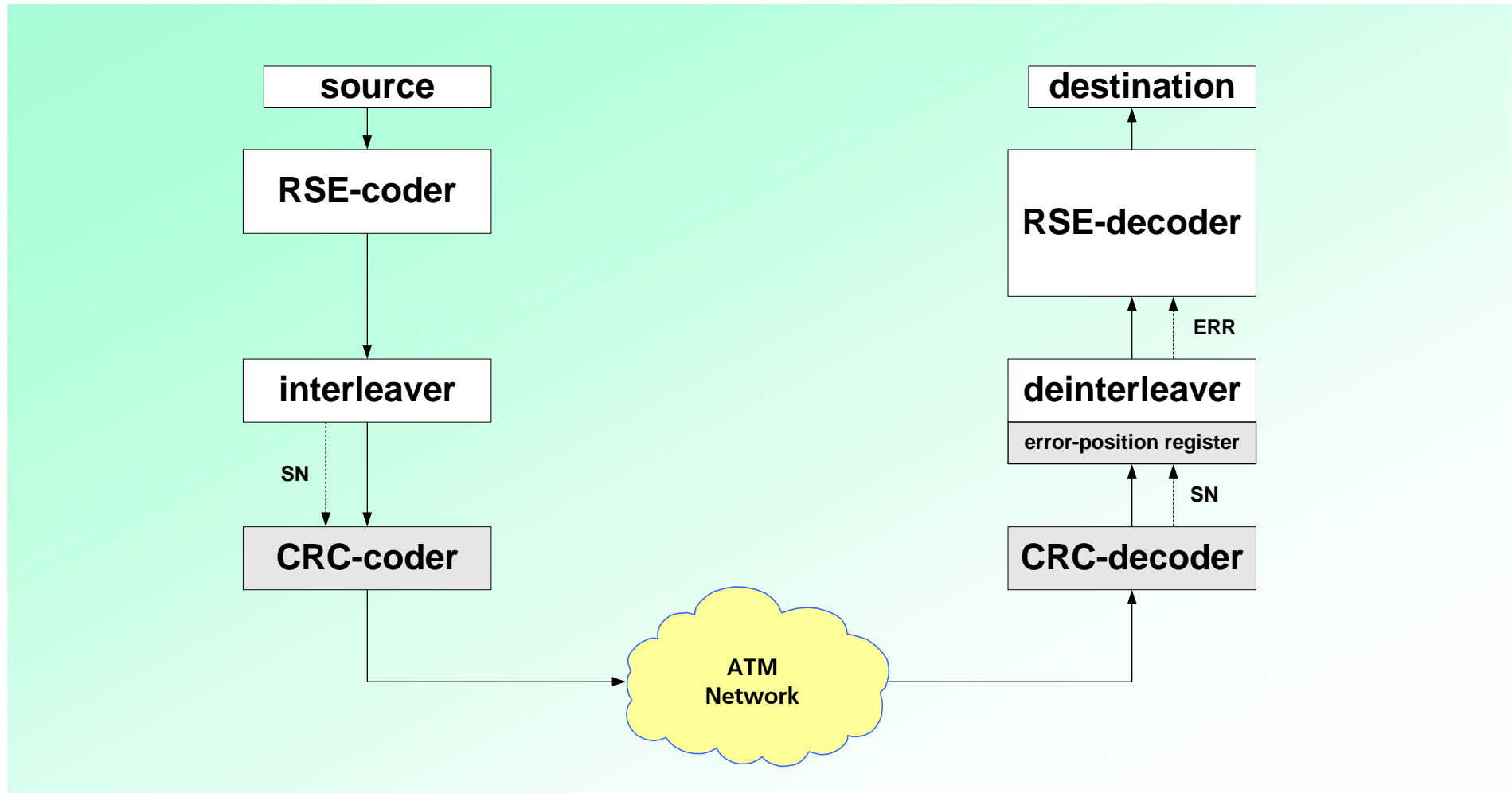
$$Z(x) = 1 + (S_1 + \sigma_1)x + (S_2 + \sigma_1 S_1 + \sigma_2)x^2 + \dots + (S_v + \sigma_1 S_{v-1} + \sigma_2 S_{v-2} + \dots + \sigma_v)x^v$$

- **Forney-Algorithm**

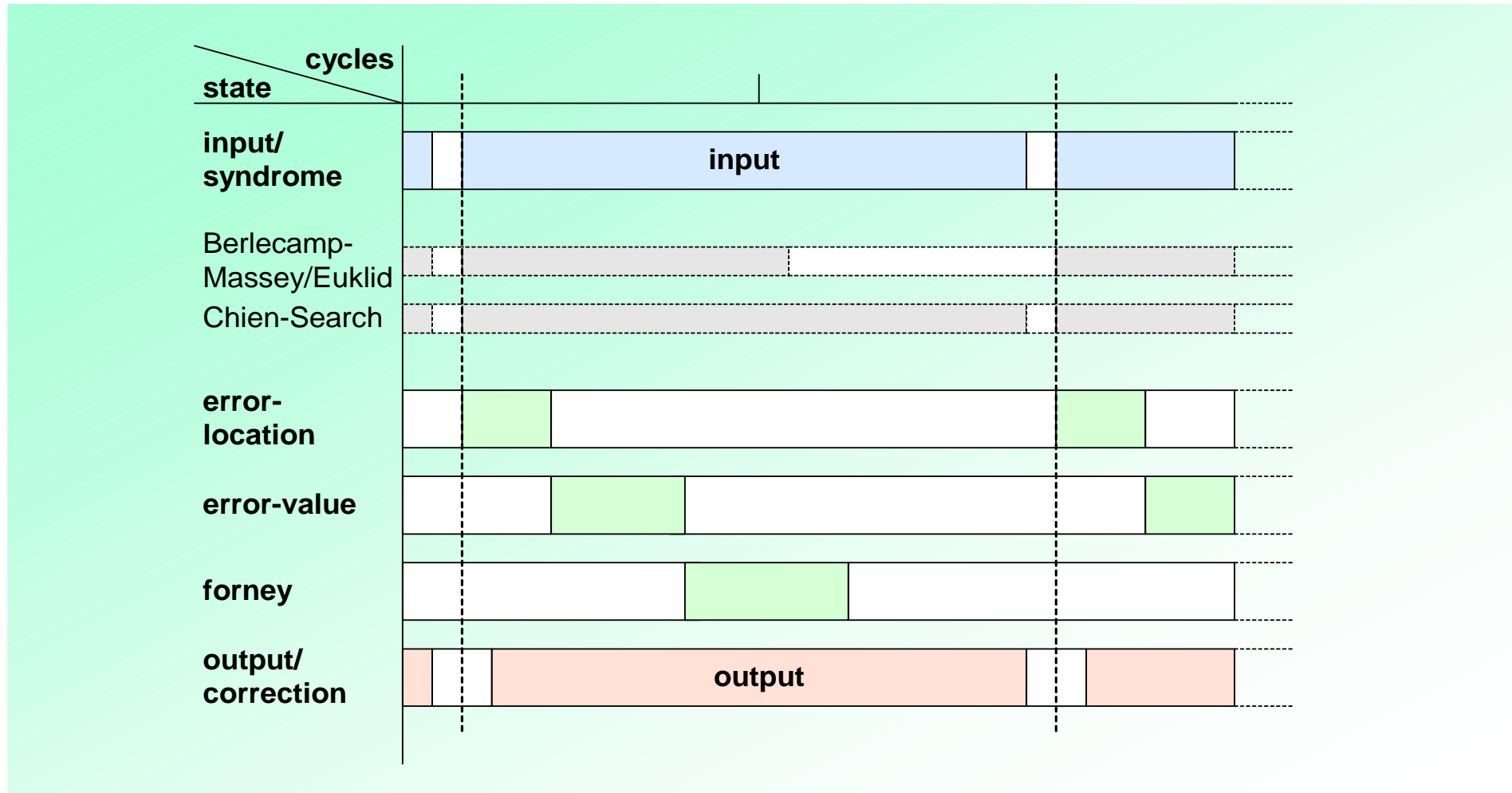
$$e_i = \frac{Z(\beta_l^{-1})}{\prod_{\substack{i=1 \\ i \neq l}}^v (1 + \beta_i \beta_l^{-1})}$$



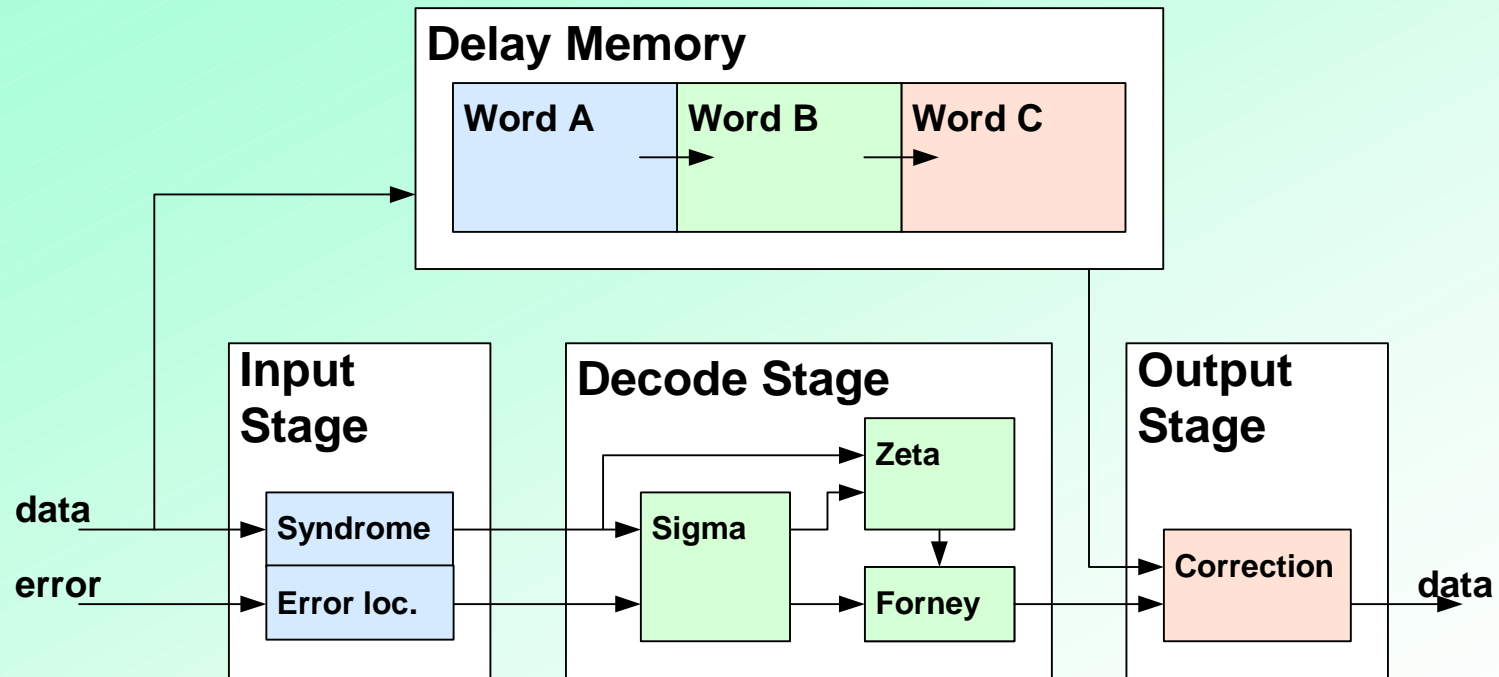
FEC based on RSE



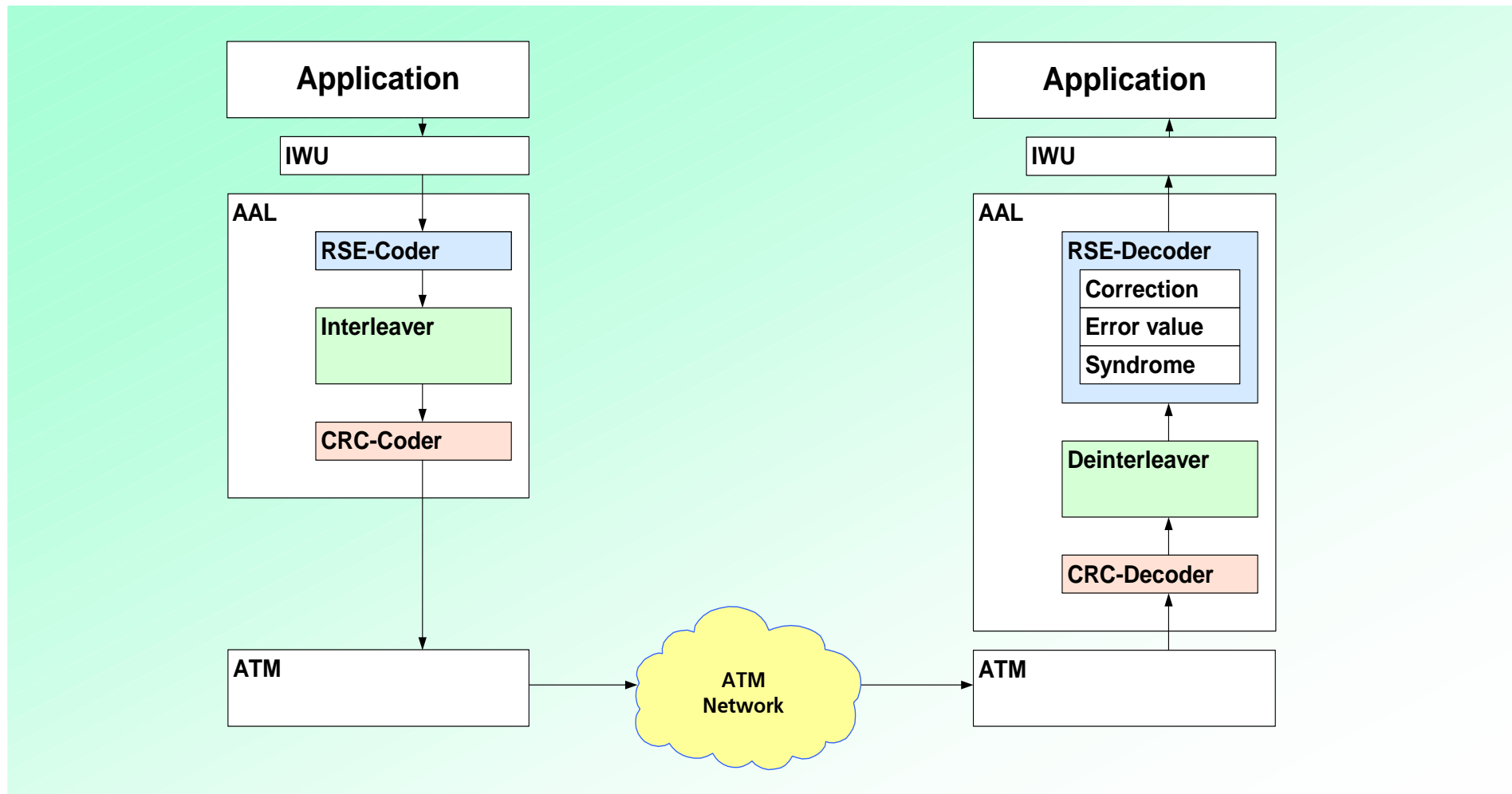
Timing Characteristic of the RSE Decoder



Pipeline Structure of the RSE Decoder



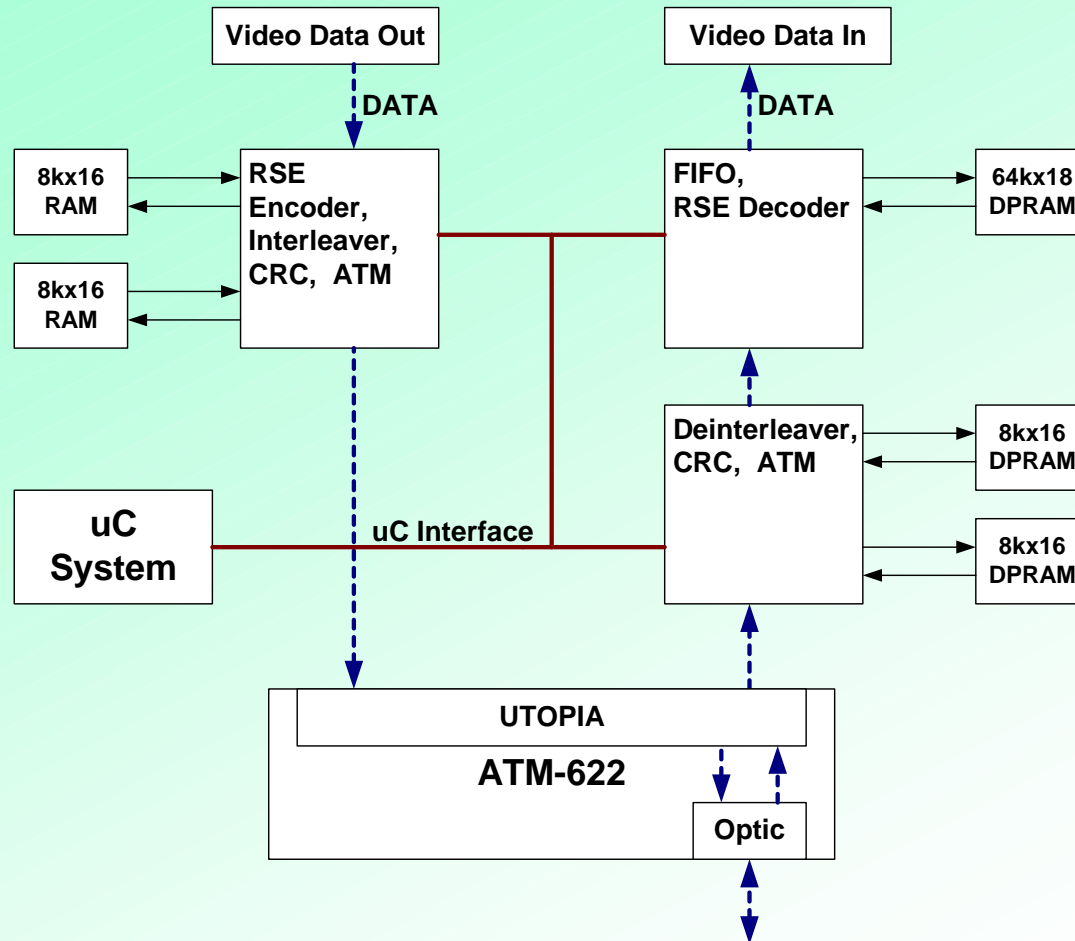
ATM System with RSE CODEC



Prototype Specification

- **Prototype based on FPGAs**
- **$(128,124,4)_2$ -RSE (3-stage pipeline)**
- **128x45 Byte Block-Interleaver**
- **4 cell-losses/corruptions per matrix correctable**
- **16 Bit data-path (bidirectional)**

System-Layout ATM Adapter



Synthesis Results

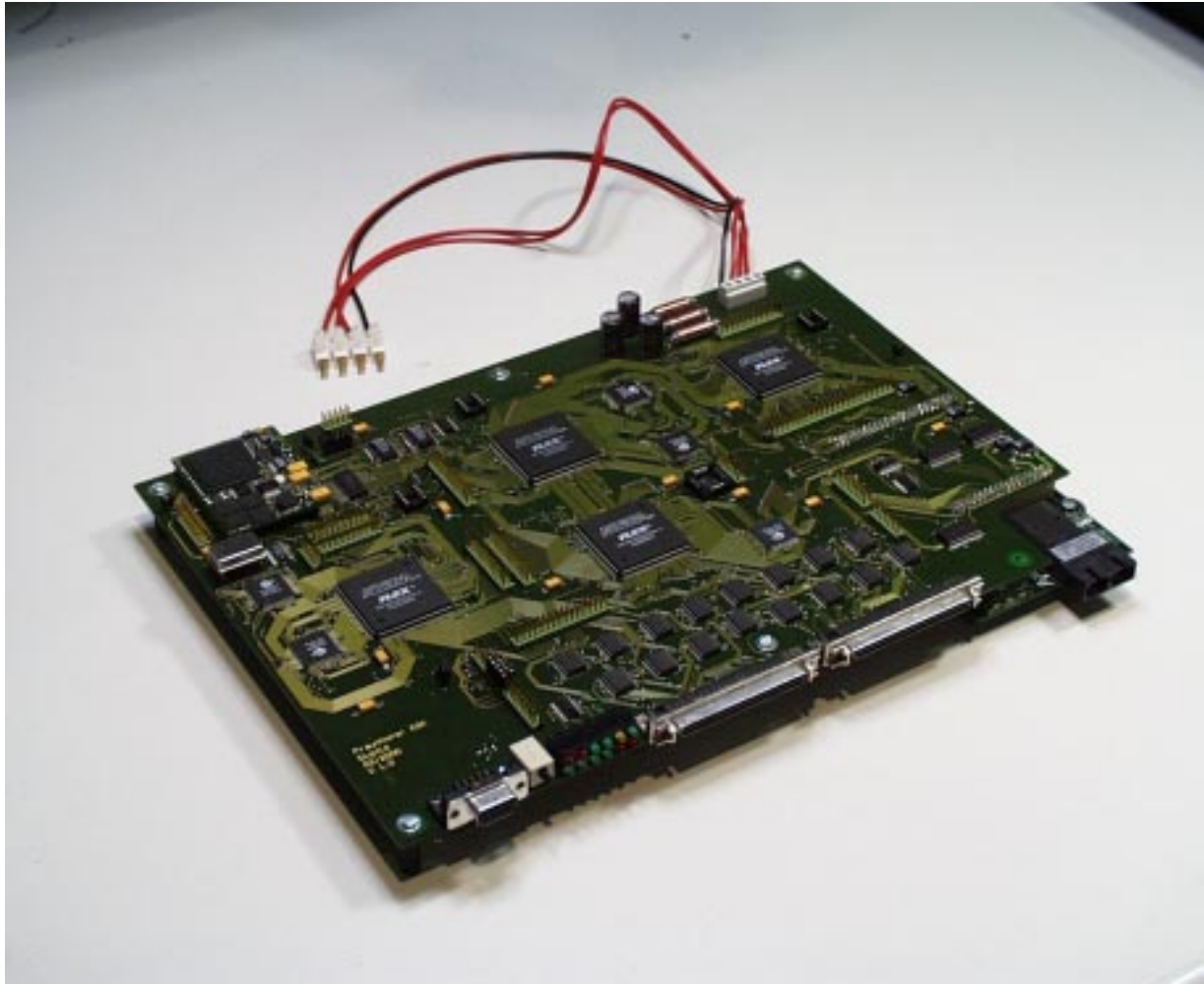
FPGA	device type, Tools	Fitting	max. clock
Encoder, Interleaver, CRC, ATM	Altera- EPF10K50EQC240-1 Synopsis Design Analyzer, Altera MAX+plus II v.9.21.	40%	37MHz
Decoder		87%	37MHz
Deinterleaver, CRC, ATM		25%	35MHz



Summary

- **RSE based FEC exploits the benefits of ATM**
- **3 stage Pipeline to handle real-time decoding**
- **Prototype with 300Mbit/s at Video IF**
- **4 cell-losses/corruptions in 6.6KBytes can be corrected**
- **ideal for high bit-rate real-time applications
e.g. Studio/Multimedia**

ATM Adapter Prototype



- 16Bit Video IF
- ATM-622 UTOPIA
- 300MBit/s at Video IF
- 25MHz System clock
- 4 cell-losses/corruptions in 6,6KByte correctable
- VBR 1:10 supported
- >2 GBit/s with 32 Bit IF and 100MHz system clock possible

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